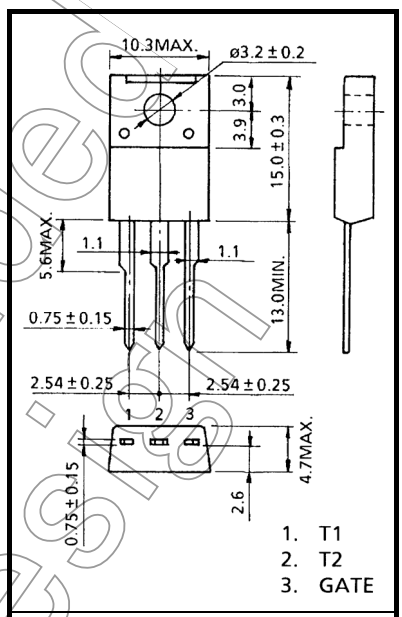
TOSHIBA BI−DIRECTIONAL TRIODE THYRISTOR SILICON PLANAR TYPE

SM10LZ47

AC POWER CONTROL APPLICATIONS

- Repetitive Peak Off−State Voltage : V_{DRM} = 800V
- R.M.S. On−State Current : $I_{T\ (RMS)}$ = 10A
- High Commutation (dv / dt)
- Isolation Voltage : V_{ISOL} = 1500V AC

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	13-10H1A

Weight: 1.7 g (typ.)

ABSOLUTE MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING	UNIT
Repetitive Peak Off−State Voltage	V_{DRM}	800	V
R.M.S On−State Current (Full Sine Waveform)	$I_{T\ (RMS)}$	10	A
Peak One Cycle Surge On−State Current (Non−Repetitive)	I_{TSM}	100 (50Hz)	A
		110 (60Hz)	
I^2t Limit Value	I^2t	50	A^2s
Critical Rate of Rise of On−State Current (Note 1)	di / dt	50	A / μs
Peak Gate Power Dissipation	P_{GM}	5	W
Average Gate Power Dissipation	$P_{G\ (AV)}$	0.5	W
Peak Gate Voltage	V_{FGM}	10	V
Peak Gate Current	I_{GM}	2	A
Junction Temperature	T_j	−40~125	°C
Storage Temperature Range	T_{stg}	−40~125	°C
Isolation Voltage (AC, t = 1min.)	V_{ISOL}	1500	V

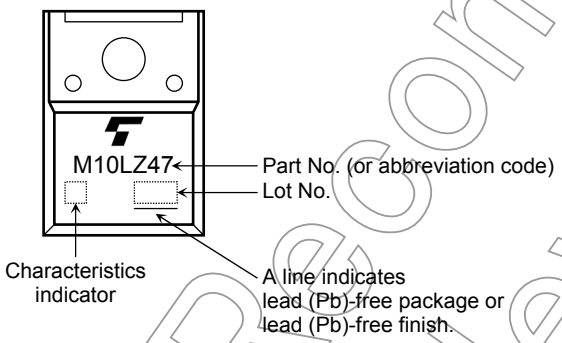
Note 1: di / dt test condition
V_{DRM} = 0.5 × Rated, $I_{TM} \leq 15A$, $t_{gw} \geq 10\mu s$,
$t_{gr} \leq 250ns$, $i_{gp} = I_{GT} \times 2.0$

Note 2: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

ELECTRICAL CHARACTERISTICS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CONDITION		MIN	TYP.	MAX	UNIT
Repetitive Peak Off−State Current		I_{DRM}	V_{DRM} = Rated		—	—	20	μA
Gate Trigger Voltage	I	V_{GT}	V_D = 12V, R_L = 20Ω	T2 (+) , Gate (+)	—	—	1.5	V
	II			T2 (+) , Gate (−)	—	—	1.5	
	III			T2 (−) , Gate (−)	—	—	1.5	
Gate Trigger Current	I	I_{GT}	V_D = 12V, R_L = 20Ω	T2 (+) , Gate (+)	—	—	30	mA
	II			T2 (+) , Gate (−)	—	—	30	
	III			T2 (−) , Gate (−)	—	—	30	
Peak On−State Voltage		V_{TM}	I_{TM} = 15A		—	—	1.5	V
Gate Non−Trigger Voltage		V_{GD}	V_D = Rated, Tc = 125°C		0.2	—	—	V
Holding Current		I_H	V_D = 12V, I_{TM} = 1A		—	—	50	mA
Thermal Resistance		$R_{th\ (j-c)}$	Junction to Case, AC		—	—	3.4	°C / W
Critical Rate of Rise of Off−State Voltage		dv / dt	V_{DRM} = 600V, T_j = 125°C Exponential Rise		—	300	—	V / μs
Critical Rate of Rise of Off−State Voltage at Commutation		(dv / dt) c	V_{DRM} = 400V, T_j = 125°C (di / dt) c = − 5.5A / ms		10	—	—	V / μs

MARKING



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